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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of
Shunpei YAMAZAKI et al.

Serial No. 09/837,877

Filed: April 19, 2001

For: Semiconductor Device

VERIFICATION OF TRANSLATION

Honorable commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

I, Kazuya Morikawa, Flat SEL A105, 304-1, Hase, Atsugi-shi, Kanagawa-ken, 243-0036, Japan, declare:

that I am well acquainted with both the Japanese and English languages; and

that to best of my knowledge and belief the following is a true and correct translation of
Japanese Patent Application No. 10-374878 filed on December 28, 1998.

I further declare that all statements made herein of my own knowledge are true and that
all statements are made on information and belief are believed to be true; and further that these
statements were made with the knowledge that willful false statements and the like so made
are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United
States Code, and that such willful false statements may jeopardize the validity of the
application or any patent issuing thereon.

Date: this 3rd day of August, 2001

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[Attachment]	Specification	1
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